4. (Amended) A compound semiconductor field effect transistor as claimed in claim 10, wherein said TiO_2 layer has a non-stoichiometric composition.

5. (Amended) A compound semiconductor field effect transistor as claimed in claim 10, wherein said compound semiconductor device further includes first and second ohmic electrodes in contact with said compound semiconductor layer at both lateral sides of said gate electrode, and wherein TiO_2 layer is provided further at an interface between said first ohmic electrode and said compound semiconductor layer and between said second ohmic electrode and said compound semiconductor layer.

6. (Amended) A compound semiconductor field effect transistor as claimed in claim 5, wherein said TiO_2 layer has a thickness allowing tunneling of carriers therethrough.

7. (Amended) A compound semiconductor field effect transistor as claimed in claim 6 wherein said TiO_2 layer is provided so as to cover a surface of said compound semiconductor layer continuously from said first ohmic electrode to said gate electrode and from said gate electrode to said second ohmic electrode.

8. (Amended) A semiconductor triode as claimed in claim 10, wherein said channel layer includes a two-dimensional electron gas.

10. (Amended) A compound semiconductor field effect transistor, comprising:

a compound semiconductor layer including a channel layer;

a gate electrode electrically contacting said compound semiconductor layer to control a current flow in said channel layer, said gate electrode having a multi-layer structure including a Ti layer, a Pt layer and an Au layer; and

an intermediate layer including a TiO_2 layer, formed between said Ti layer and said compound semiconductor layer.

Please ADD new claims 11 - 13 to read as follows:

11. (New) The compound semiconductor field effect transistor as claimed in claim 10, wherein said compound semiconductor layer comprises an InGaAs layer acting as said channel layer and an electron-supplying layer of InAlAs formed on said channel layer, and wherein said intermediate layer is formed between said Ti layer and said InAlAs layer.

12. (New) The compound semiconductor transistor as claimed in claim 11, wherein said multi-layer structure comprises a layered structured in which a Pt layer and an Au layer are stacked on said Ti layer.

13. (New) The compound semiconductor field effect transistor as claimed in claim 10, wherein said TiO_2 layer is an insulating layer.